CLAIMS

What is claimed is:

1) A system for reducing power in memory cells comprising:

a) a circuit, the circuit having an input and an output;

b) wherein the input is connected to a wordline of the memory cells;

c) wherein the output is connected to a positive voltage supply node of the memory cells;

d) wherein a first voltage applied to the output is reduced by at least one V_t from a supply voltage, VDD, when the wordline is inactive;

e) wherein a second voltage applied to the output is near the supply voltage, VDD, when the wordline is active.

2) The system as in Claim 1 wherein the memory cells are SRAM cells.

3) The system as in Claim 1 wherein the memory cells are DRAM cells.

4) The system as in Claim 1 wherein the circuit comprises:

a) an inverter, the inverter having an input and an output;

b) an NFET, the NFET having a gate, a drain, and a source;

c) a PFET, the PFET having a gate, a drain, and a source;

d) wherein the input of the inverter is connected to the input of the circuit;

e) wherein the output of the inverter is connected to the gate of the PFET;

f) wherein the source of the PFET, the gate of the NFET, and drain of the NFET are connected to the supply voltage, VDD;

g) where in drain of the PFET and the source of the NFET are connected to the output of the circuit.

5) A system as in Claim 1 wherein the circuit comprises:

a) a first NFET, the first NFET having a gate, a drain, and a source;

b) a second NFET, the second NFET having a gate, a drain, and a source;

c) a third NFET, the third NFET having a gate, a drain, and a source;

d) a fourth NFET, the fourth NFET having a gate, a drain, and a source;

e) wherein the gate of the first NFET is connected to the input of the circuit;

f) wherein the drain and the source of the first NFET is connected to the source of the second NFET and to the gate of the third NFET;

g) wherein the drain of the second NFET, the gate of the second NFET, the drain of the third NFET, the drain of the fourth NFET, and the gate of the fourth NFET are connected to the supply voltage, VDD;

h) wherein the source of the third NFET, and the source of the fourth NFET are connected to the output of circuit.

6) A system for reducing power in memory cells comprising:

a) a circuit, the circuit having an input, a first output, and a second output;

b) wherein the input is connected to an active-low wordline;

c) wherein the first output is connected to a local wordline of the memory cells;

d) wherein the second output is connected to a positive voltage supply node of the memory cells;

e) wherein a first voltage applied to the second output is reduced by at least one V_t from a supply voltage, VDD, when the active-low wordline is high;

f) wherein a second voltage applied to the second output is near the supply voltage, VDD, when the active-low wordline is low.

7) The system as in Claim 6 wherein the circuit comprises:

a) an inverter, the inverter having an input and an output;

b) an NFET, the NFET having a gate, a drain, and a source;

c) a PFET, the PFET having a gate, a drain, and a source;

d) wherein the input of the inverter is connected to the input of the circuit;

e) wherein the output of the inverter is connected to the first output of the circuit;

f) wherein the source of the PFET, the gate of the NFET, and drain of the NFET are connected to the supply voltage, VDD;

g) wherein drain of the PFET and the source of the NFET are connected to the second output of the circuit.

8) A method for manufacturing a circuit for reducing power in memory cells comprising:

a) fabricating an inverter, the inverter having an input and an output;

b) fabricating an NFET, the NFET having a gate, a drain, and a source;

c) fabricating a PFET, the PFET having a gate, a drain, and a source;

d) wherein the input of the inverter is connected to a wordline of the memory cells;

e) wherein the output of the inverter is connected to the gate of the PFET;

f) wherein the source of the PFET, the gate of the NFET, and drain of the NFET are connected to the supply voltage, VDD;

g) where in drain of the PFET and the source of the NFET are connected to a positive voltage supply node of the memory cells.

9) A method for manufacturing a circuit for reducing power in memory cells comprising:

a) fabricating a first NFET, the first NFET having a gate, a drain, and a source;

b) fabricating a second NFET, the second NFET having a gate, a drain, and a source;

c) fabricating a third NFET, the third NFET having a gate, a drain, and a source;

d) fabricating a fourth NFET, the fourth NFET having a gate, a drain, and a source;

e) wherein the gate of the first NFET is connected to the wordline of the memory cells;

f) wherein the drain and the source of the first NFET is connected to the source of the second NFET and to the gate of the third NFET;

g) wherein the drain of the second NFET, the gate of the second NFET, the drain of the third NFET, the drain of the fourth NFET, and the gate of the fourth NFET are connected to the supply voltage, VDD;

h) wherein the source of the third NFET, and the source of the fourth NFET are connected to a positive voltage supply node of the memory cells.

10) A method for manufacturing a circuit for reducing power in memory cells comprising:

a) fabricating an inverter, the inverter having an input and an output;

b) fabricating an NFET, the NFET having a gate, a drain, and a source;

c) fabricating a PFET, the PFET having a gate, a drain, and a source;

d) wherein the input of the inverter is connected to an active low wordline;

e) wherein the output of the inverter is connected to a local wordline of the memory cells;

f) wherein the source of the PFET, the gate of the NFET, and drain of the NFET are connected to the supply voltage, VDD;

g) wherein drain of the PFET and the source of the NFET are connected to a positive voltage supply node of the memory cells.